Portable CD 1996

Service
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KEY COMPONENTS
BATTERY CHARGING
DC/DC-CONVERTER

System Description

ESA
ESP

COMPACT disc DIGITAL AUDIO

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INTRODUCTION

The booklet on hand describes the most important innovations and changes in the world of portable CD for the year of 1996.
It should be seen as an addendum to the "System Description Portable CD ´94" – 4822 725 24941.
Because some chapters of this addendum refer to basics, already described in the above mentioned booklet, the user should take care to have both manuals available.

Contents of the System Description Portable CD ´94
- Principles of shock absorbing CD-players
- Compact disc mechanism CDM12.3B/CDM12.3BL
- Key components
  - HF-amplifier TDA1302
  - Digital servo controller TDA1301T
  - Signal processor SAA7345
  - Shock absorbing RAM addresser SAA7346
  - D/A-converter TDA1345, TDA1305T
- Wired remote control system

The booklets are written for service trainee and everybody who wants to get rid of the basics behind. They cover both, fundamentals and new technologies in portable CD-players.

The ´94 edition mainly refers to circuit diagrams of the so-called "HILLARY-range", a product family that consists of the typenumbers AZ683x, AZ684x and AZ685x.
The ´96 edition refers to circuit diagrams of the "SHARON-range", typenumbers AZ726x, AZ736x and AZ746x.

CDM12.3BLC – COMPACT DISC DRIVE

The CDM12.3BLC is the successor of the CDM12.3BL, further optimized for low power consumption.
Just as the CDM12.3BL a two stage three spot system with single foucault focus error detection and an integrated optical pick-up is used.
For description of lightpath, focus error detection and radial tracking see chapter “CDM12.3B” of booklet “Portable CD ´94”.

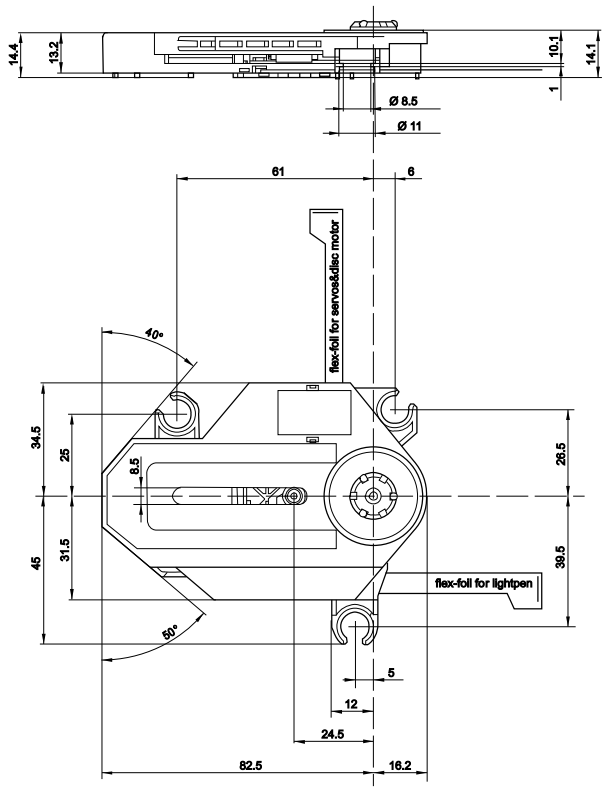
Technical specification CDM12.3BLC

Focus/radial tracking actuator	CDM12.3BLC
Working area:	
focus	±0.5mm
radial tracking	0.35mm min.
DC sensitivity:	
focus	1mm/V ±20%
radial tracking	0.24mm/V ±20%
AC sensitivity (200Hz):	
focus	0.16N/A ±20%
radial tracking	0.25N/A ±20%
Resonance frequency:	
focus	30Hz +7Hz
radial tracking	49Hz ±5Hz
Coil resistance:	
focus	7.1Ω ±15%
radial tracking	18Ω ±15%
Laser diode	
Laser wavelength (30°C)	780nm ±20nm
Max. power intensity out of lens	≤0.5mW
Nom. laser current	36mA (47mA max.)
Slide motor	
Motor type	FF-030PK-08250
Resistance (20°C)	13.8Ω ±10%
Starting voltage in application	0.6V typ. (1.2V max.)
Disc readout diameter	47.4...117.5mm
Turntable motor	
Motor type	RF-410CH-12250
Resistance (20°C)	5.7Ω ±8%
Operating voltage in application	0.5V typ.

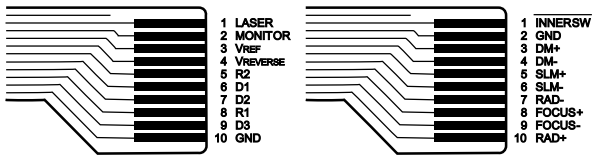
Handling recommendations

- Storage in dusty environments should be avoided.
- To avoid damage of the LDGU by electrostatic discharges, measuring equipment and operators should be grounded during handling.
- Contamination of the objective lens will influence the performance. Avoid fingerprints on the lens, handle the CDM in a clean environment.
- The actuator with lightpath has been adjusted carefully during manufacturing. Avoid high forces on this part. Do not disassemble or re-adjust.
- The laserbeam may damage the human eye. Do not look directly into the objective lens.
- Fast heating up (e.g. by bringing the CDM from a cold place into a warm and humid room) can result in moisture condensating on the lens thus influencing the playability for a certain time. Before checking the performance the CDM should stabilize for at least 30 minutes.

Mechanical dimensions



Flex-foils for lightpen, servos & disc motor



Foil for lightpen

Foil for servos & disc motor

SAA7372GP – CD-DECODER & DIGITAL SERVO IC "CD7"

GENERAL DESCRIPTION

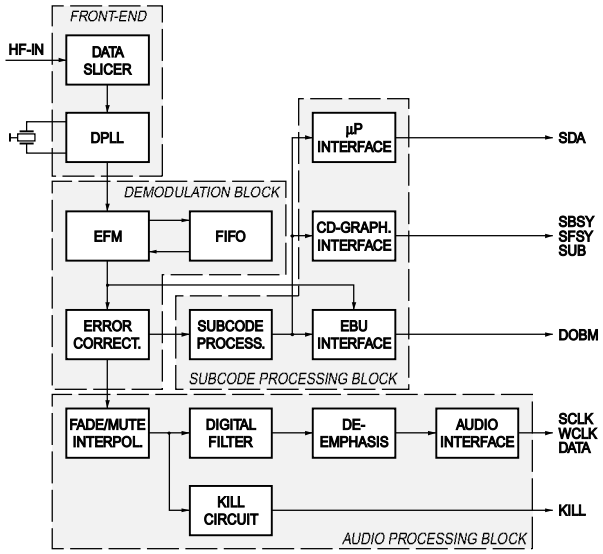
The CD7 is a single chip combining the functions of a CD-decoder and a digital servo controller. The decoder part of the CD7 is based on the SAA7345GP (CD6), with an improved error correction strategy. The digital servo part of the CD7 is based on the TDA1301 (DSIC2), with improved performance.

FUNCTIONAL DESCRIPTION DECODER PART

The decoder part of the CD7 has the following features:

- Single and double speed mode
- Lock to disc mode
- On-chip clock multiplier allows use of 8.4672MHz crystal
- Data slicer and clock generator
- Demodulator
- Subcode data processing
- FIFO and full error corrector (t=2, e=4)
- Audio processing block (incl. oversampling)
- DAC, EBU and CD-graphics interface
- Versatile pins interface
- Spindle motor control

Data flow within the decoder part



Crystal oscillator and decoder speed

The oscillator of the CD7 is a conventional two pin design, running at 8...35MHz. It is capable of operating with both, crystals and ceramic resonators, as well as fundamental and third overtone crystals.
Normal oscillation frequencies required are 8.4672MHz, 16.9344MHz, or 33.8688MHz depending on the internal clock settings and usage of the internal clock multiplier PLL. Two decoder speeds are possible on the SAA7372.

Data slicer and clock regenerator

The CD7 has an integrated slice level comparator which is clocked by one of the three crystal oscillator frequencies. The slice level is controlled by an internal current source applied to an external capacitor.
Regeneration of the bit clock is done with an internal fully digital PLL. No external components are required. The DPLL has two control registers for bandwidth and equalization (see section "CD7 decoder register list").

Demodulator

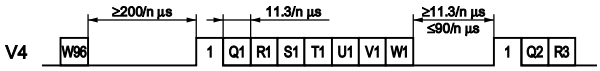
The demodulator decodes the 14bit EFM data and subcode words into 8bit symbols. It also incorporates an RL2 error correction circuit. Every symbol detected as RL2 will be will be pushed back to RL3. To do this the phase error of both EFM edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

Subcode data processing

The 96bit Q-channel word is stored in an internal buffer. The last 16bits are used to internally to perform a CRC. If the data is good, SUBQREADY-I signal will go LOW.
SUBQREADY-I can be read via the status signal if selected by status control register (see section "CD7 decoder register list"). Q-channel data can also be read via the µP-interface.

Subcode interface V4

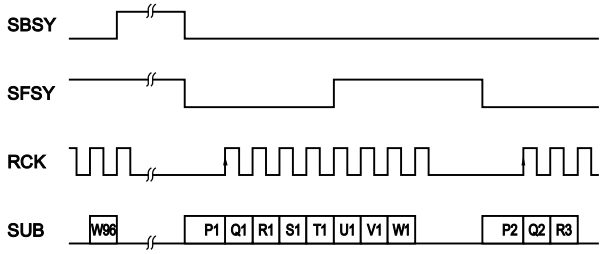
Data from the subcode channels Q...W can be read via the V4-pin if selected by the versatile pins register (see section "CD7 decoder register list"). The format is similar to RS232, as shown below.



The subcode sync word is formed by a minimum pause of 200/n µs. Each subcode byte starts with a "1" followed by 7bits (Q...W). The gap between bytes is variable between 11.3/n µs and 90/n µs.
Subcode data is also available in the EBU output of the CD7 (DOBM-pin) in a similar format.

CD-graphics interface

Data from the subcode channels P...W can be read via the CD-graphics interface which conforms to EIAJ CP-2401.
The interface is enabled and configured as either a 3-wire or 4-wire interface by the CD-graphics interface register (see section "CD7 decoder register list").
The output format of the interface is shown below.



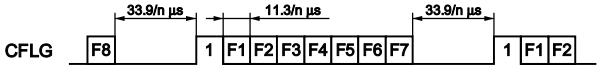
Remark: The RCK clock signal is supplied by another device such as a CD-graphics decoder.

FIFO and error corrector

The CD7 has an internal ±8 frame FIFO buffer, used to cover speed deviations of the turntable motor. If an overflow occurs during playback (e.g. as result of a rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator will be activated in order to minimize the effect of data loss (see section "Error concealment").
The error corrector is a t=2, e=4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) data frames. Four symbols are used from each frame as parity symbols. This error correction algorithm can correct up to two errors on C1 level and up to four errors on C2 level (that is the maximum level of error correction available).
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector can not ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM-pin) and the EF-output with I2S for CD-ROM applications.

Flags output CFLG
The flags output pin CFLG (open drain) shows the status of the error corrector and interpolator. It is updated every frame (7.35*n kHz). The output format is shown below.



The different flags have the following meanings:

F1	F2	F3	F4	F5	F6	F7	F8	FUNCTION
0	X	X	X	X	X	X	X	No absolute time sync
1	X	X	X	X	X	X	X	Absolute time sync
X	0	0	X	X	X	X	X	C1 frame contained no errors
X	0	1	X	X	X	X	X	C1 frame contained 1 error
X	1	0	X	X	X	X	X	C1 frame contained 2 errors
X	1	1	X	X	X	X	X	C1 frame uncorrectable
X	X	X	0	0	X	X	0	C2 frame contained no errors
X	X	X	0	0	X	X	1	C2 frame contained 1 error
X	X	X	0	1	X	X	0	C2 frame contained 2 errors
X	X	X	0	1	X	X	1	C2 frame contained 3 errors
X	X	X	1	0	X	X	0	C2 frame contained 4 errors
X	X	X	1	1	X	X	1	C2 frame uncorrectable
X	X	X	X	X	0	0	X	No interpolations
X	X	X	X	X	0	1	X	At least one 1-sample interpolation
X	X	X	X	X	1	0	X	At least one hold and no interpolations
X	X	X	X	X	1	1	X	At least one hold and one 1-sample int.

EBU interface
The digital output signal at the DOBM-pin of the CD7 is according the IEC958 specification. The format consists of 32bit words (so called "subframes"), transmitted in biphase mark code (two transitions for a logic "1" and one transition for a logic "0"). Subframes are transmitted in blocks of 384. The 32bits of one subframe have the following meaning:

BIT No	NAME	FUNCTION
0...3	sync	sync word B, M or W (see below)
4...7	auxiliary	not used (normally zero)
8...27	audio sample	2´s compliment, MSB=bit 27
28	validity flag	valid="0"
29	user data	used for subcode data Q...W
30	channel status	control bits and category code
31	parity bit	even parity for bits 4...30

Sync word
The sync word is formed by violation of the biphase rule and does not contain any data. It is used for synchronization. The length is equivalent to 4 data bits. Three different sync patterns indicate the following situations:
SyncB : Start of a new block, audio sample=left channel
SyncM : Start of a new subframe, audio=left channel
SyncM : Start of a new subframe, audio=right channel

Audio sample
Left and right audio channels are transmitted alternately.

Validity flag
The validity flag indicates uncorrectable audio samples. This flag remains the same even if data is taken after error concealment.

User data
The user data carries the subcode bits Q...W. User data is transmitted asynchronous with the block rate.

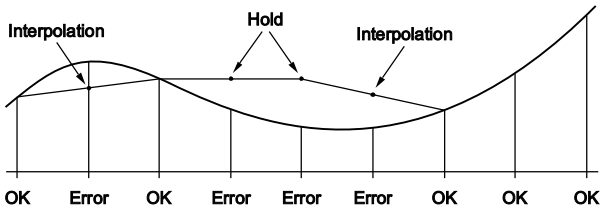
Channel status
The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The bit assignment is shown in the table below:

BIT No	NAME	FUNCTION
0...3	control	copy of checked Q-channel bits 0...3 bit2="1": copy permitted bit3="1": recording has pre-emphasis
4...7	reserved	always zero
8...15	category code	CD: bit8="1", all other bits="0"
16...27	reserved	always zero
28...29	clock accuracy	set by EBU control register "00"=level II, "01"=level III, "10"=level I
30...191	reserved	always zero

The CD7 has three different EBU modes, selectable via the EBU output format register (see section "CD7 decoder register list").

Audio functions

Error concealment
A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. Left and right channels have independent interpolators. The erroneous sample is replaced by a level midway between the preceding and following sample. If more than one consecutive uncorrectable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample.



In CD-ROM modes error concealment is not executed.

De-emphasis and phase linearity
When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase linearity of the digital oversampling filter to ≤ ±1° within the band 0...16kHz. With de-emphasis the filter is not phase linear. If the de-emphasis signal is set to be available at the V5-pin of the versatile pins interface (see section "CD7 decoder register list"), the de-emphasis filter is bypassed and an external circuit can be used.

Digital oversampling filter
The CD7 includes a 2 to 4 times oversampling IIR-filter. Oversampling is selected via the DAC mode chosen (see section "DAC interface").
The filter specification of the 4 times oversampling filter is given in the table below:

PASSBAND	ATTENUATION
0...19kHz	≤0.001dB
19...20kHz	≤0.03dB
STOPBAND	ATTENUATION
24kHz	≥25dB
24...27kHz	≥38dB
27...35kHz	≥40dB
35...64kHz	≥50dB
64...68kHz	≥31dB
68kHz	≥35dB
69...88kHz	≥40dB

The attenuations do not include the sample and hold at the DAC output or the DAC post filter.
When using the oversampling filter, the output level is scaled -0.5dB down, to avoid overflow on full-scale sinewave inputs (0...20kHz).

Mute, attenuation and fade
The CD7 incorporates a digital level controller which performs the functions of soft mute, attenuation and fade. The features are selectable via the fade and attenuation register (see section "CD7 decoder register list").

Mute
The mute command ramps the audio signal level to zero in a maximum of 128 steps (depending on the current position of the fade counter). Ramping from full scale to zero level takes 3/n ms.

Attenuate
The attenuate command scales the audio signal level to -12dB of full scale.

Fade
Fade activates a 128 stage counter which allows the audio signal level to be scaled up/down. The fade counter is controlled by the stepup/stepdown commands. If the fade level is controlled in a continuous way, a pause of at least 22/n ms must take place between any two stepup or stepdown commands.

Full scale
The full scale command ramps the audio signal level back to full scale. Ramping from mute to full scale takes 3/n ms.

Peak detector
The peak detector of the CD7 measures the highest audio level (absolute value) on positive peaks for the left and right channel. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81...88 contain the left peak value (bit88=MSB), and bits 89...96 contain the right peak value (bit96=MSB). The values are reset after reading the Q-channel data via the µP-interface.

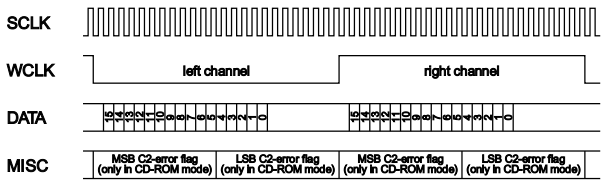
Kill circuit
The kill circuit detects digital silence by testing for an all-zero or all-ones data words in the left or right channel before the digital filter. The output is switched LOW if silence has been detected for at least 250ms. When mute is active, or CD7 is in CD-ROM mode, the kill output is forced LOW.

DAC interface
The CD7 is compatible with a wide range of D/A converters. The supported formats are shown in the table below:

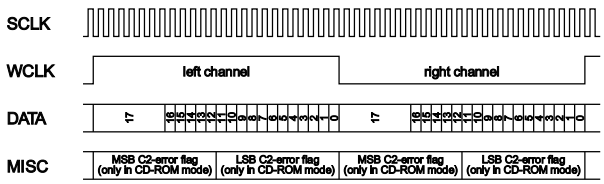
REG.	fs	BITS	SCLK [MHz]	FORMAT	INTERPOL.
1010	fs	16	2.1168∗n	I^2S CD-ROM mode	no
1011	fs	16	2.1168∗n	EIAJ CD-ROM mode	no
110X	4fs	18	8.4672∗n	I^2S - 18bit	yes
1111	2fs	16	4.2336∗n	I^2S - 18bit	yes
1110	fs	16/18	2.1168∗n	I^2S - 16/18bit	yes
000X	4fs	16	8.4672∗n	EIAJ - 16bit	yes
0011	2fs	16	4.2336∗n	EIAJ - 16bit	yes
0010	fs	16	2.1168∗n	EIAJ - 16bit	yes
010X	4fs	18	8.4672∗n	EIAJ - 18bit	yes
0111	2fs	18	4.2336∗n	EIAJ - 18bit	yes
0110	fs	18	2.1168∗n	EIAJ - 18bit	yes

All formats are MSB first. The sampling frequency fs depends on the disc speed n and is 44.1kHz in single speed mode and 88.2kHz in double speed mode. The polarity of the word clock WCLK and the audio data can be inverted via the DAC output register (see section "CD7 decoder register list").

I2S-data format (16bit word length shown)



EIAJ-data format (18bit word length shown)



Turntable motor control
The turntable motor is controlled by an integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by the motor output configuration register (see section "CD7 decoder register list"), are supported:
- PDM-output – 2-line, 1∗n MHz sampling frequency
- PWM-output – 2-line, 22.05∗n kHz modulation frequency
- PWM-output – 4-line, 22.05∗n kHz modulation frequency
- CDV mode

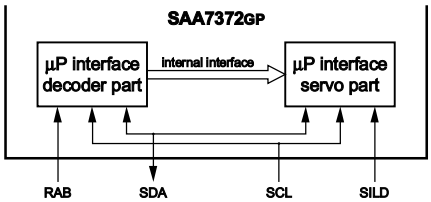
CD7-communication modes

The CD7 provides three different methods for transferring data to and from the IC. These are:

- 4-wire mode
- 3-wire mode
- I2C mode

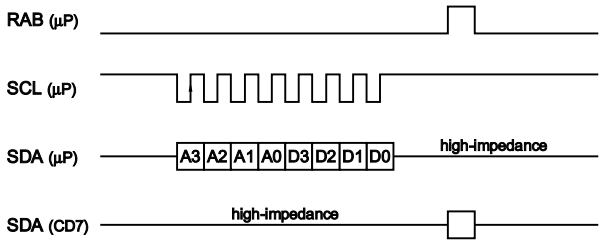
4-wire mode

This mode is backwards compatible to the “shared” 4-wire communication bus used for CD6 and DSIC2. The bus uses common serial bit clock (SCL) and serial data (SDA) for both servo and decoder parts. However, each part has a separate strobe line – SILD for the servo part and RAB for the decoder part.

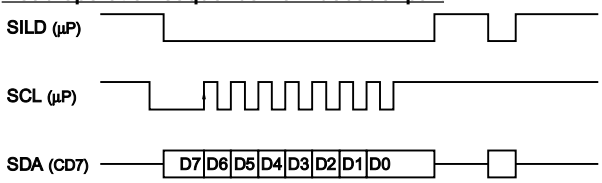


The internal interface between servo and decoder part must be disabled in order to allow direct communication to the decoder part.

Write operation sequence to decoder part

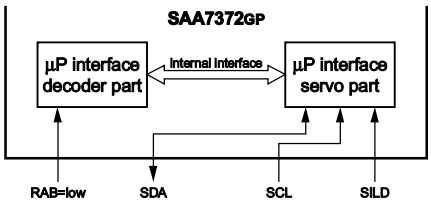


Read operation sequence from decoder part



3-wire mode

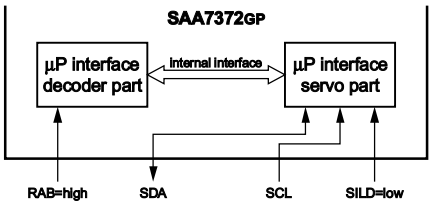
The 3-wire mode is very similar to the 4-wire mode, except that all communications to the decoder is done via the servo part. Communication to the servo uses the same hardware protocol and timings as for 4-wire mode.



Extra servo commands exist for write and read access to the decoder via the internal interface. The internal interface must be enabled. RAB is not used and must be LOW.

I2C mode

I2C mode is selected by forcing the condition RAB=HIGH and SILD=LOW.



As with 3-wire mode, all communication to the decoder is made via the servo part. In this mode the internal interface is permanently enabled.

The command protocol used is virtually identical to that of 3-wire mode, except that the respective CD7 slave address (read or write) must be transmitted before the command byte is sent.

CD7 decoder register list

The tables below show the registers of the decoder part of the CD7.

1. Fade and attenuation register

REGISTER	ADDR.	DATA	FUNCTION
Fade&Attenuation	0000	X000	Mute
		X01X	Attenuate
		X001	Full scale
		X100	Step down
		X101	Step up

2. Motor mode register

REGISTER	ADDR.	DATA	FUNCTION
Motor mode	0001	X000	Motor off mode
		X001	Motor stop mode1
		X010	Motor stop mode2
		X011	Motor start mode1
		X100	Motor start mode2
		X101	Motor jump mode
		X111	Motor play mode
		X110	Motor jump mode1
		1XXX	Anti-windup active
		0XXX	Anti-windup off

3. Status control register

REGISTER	ADDR.	DATA	FUNCTION
Status control	0010	0000	Status=SUBQREADY-I
		0001	Status=MOTSTART1
		0010	Status=MOTSTART2
		0011	Status=MOTSTOP
		0100	Status=PLL LOCK
		0101	Status=V1
		0110	Status=V2
		0111	Status=MOTOR-OV
		1X00	Status=FIFO overflow
		1X01	Status=shock detect
		1X10	Status=latched shock detect
		1X11	Status=latched shock reset

4. DAC output format register

REGISTER	ADDR.	DATA	FUNCTION
DAC output	0011	1010	I^2S CD-ROM mode
		1011	EIAJ CD-ROM mode
		110X	I^2S - 18bit, 4fs
		1111	I^2S - 18bit, 2fs
		1110	I^2S - 16bit, fs
		000X	EIAJ - 16bit, 4fs
		0011	EIAJ - 16bit, 2fs
		0010	EIAJ - 16bit, fs
		0100	EIAJ - 18bit, 4fs
		0111	EIAJ - 18bit, 2fs
		0110	EIAJ - 18bit, fs

5. Motor gain register

REGISTER	ADDR.	DATA	FUNCTION
Motor gain	0100	X000	Motor gain G=3.2
		X001	Motor gain G=4.0
		X010	Motor gain G=6.4
		X011	Motor gain G=8.0
		X100	Motor gain G=12.8
		X101	Motor gain G=16.0
		X110	Motor gain G=25.6
		X111	Motor gain G=32.0
		0XXX	Disable comp. clock divider
		1XXX	Enable comp. clock divider only if SELPLL=high

6. Motor bandwidth register

REGISTER	ADDR.	DATA	FUNCTION
Motor bandwidth	0101	XX00	Motor f4=0.5*n Hz
		XX01	Motor f4=0.7*n Hz
		XX10	Motor f4=1.4*n Hz
		XX11	Motor f4=2.8*n Hz
		00XX	Motor f3=0.85*n Hz
		01XX	Motor f3=1.71*n Hz
		10XX	Motor f3=3.42*n Hz

7. Motor output configuration register

REGISTER	ADDR.	DATA	FUNCTION
Motor output configuration	0110	XX00	Motor power maximum 37%
		XX01	Motor power maximum 50%
		XX10	Motor power maximum 75%
		XX11	Motor power maximum 100%
		00XX	MOTO1, MOTO2 pins 3-state
		01XX	Motor PWM mode
		10XX	Motor PDM mode
		11XX	Motor CDV mode

8. DAC output and status control register

REGISTER	ADDR.	DATA	FUNCTION
DAC output and status control	0111	XX0X	Interrupt signal from servo at STATUS pin
		XX1X	Status bit from decoder status register at STATUS pin
		X0XX	DAC data normal value
		X1XX	DAC data inverted value
		0XXX	Left channel first at DAC
		1XXX	Right channel first at DAC

9. PLL loop filter bandwidth register

REGISTER	ADDR.	DATA	FUNCTION		
			Loop BW [Hz]	Internal BW [Hz]	Low pass BW [Hz]
PLL loop filter bandwidth	1000	0000	1640*n	525*n	8400*n
		0001	3279*n	263*n	16800*n
		0010	6560*n	131*n	33600*n
		0100	1640*n	1050*n	8400*n
		0101	3279*n	525*n	16800*n
		0110	6560*n	263*n	33600*n
		1000	1640*n	2101*n	8400*n
		1001	3279*n	1050*n	16800*n
		1010	6560*n	525*n	33600*n
		1100	1640*n	4200*n	8400*n
		1101	3279*n	2101*n	16800*n
		1110	6560*n	1050*n	33600*n

10. PLL loop filter equalization register

REGISTER	ADDR.	DATA	FUNCTION
PLL loop filter equalization	1001	0001	PLL 30ns over-equalization
		0010	PLL 15ns over-equalization
		0011	PLL nominal equalization
		0100	PLL 15ns under-equalization
		0101	PLL 30ns under-equalization

11. EBU output format register

REGISTER	ADDR.	DATA	FUNCTION
EBU output	1010	XX0X	EBU data before concealm.
		XX1X	EBU data after conc. & fade
		X0X0	Level II clock acc. (<1000ppm)
		X0X1	Level I clock acc. (<50ppm)
		X1X0	Level III clock acc. (>1000ppm)
		X1X1	EBU off - output low
		0XXX	Flags in EBU off
		1XXX	Flags in EBU on

12. Speed control register

REGISTER	ADDR.	DATA	FUNCTION
Speed control	1011	X0XX	33.8688MHz crystal present or 8.4672MHz crystal with SELPLL=high
		X1XX	16.9344MHz crystal present
		0XXX	Single speed mode
		1XXX	Double speed mode
		XX00	Standby1: CD-STOP mode
		XX10	Standby2: CD-PAUSE mode
		XX11	Operating mode

13. Versatile pins register

REGISTER	ADDR.	DATA	FUNCTION
Versatile pins interface	1100	XXX1	External offtrack input at V1
		XXX0	Internal offtrack signal used
		XX0X	Kill-Left at KILL-output, Kill-Right at V3-output
		X01X	V3 = 0 - single kill output
		X11X	V3 = 1 - single kill output

14. Versatile pins register

REGISTER	ADDR.	DATA	FUNCTION
Versatile pins interface	1101	0000	4-line motor (using V4, V5)
		XX01	Q...W subcode at V4
		XX10	V4 = 0
		XX11	V4 = 1
		01XX	de-emphasis signal at V5
		10XX	V5 = 0
		11XX	V5 = 1

15. Versatile pins register

REGISTER	ADDR.	DATA	FUNCTION
Versatile pins interface	1110	00XX	Audio features disabled
		01XX	Audio features enabled
		0X0X	Lock to disc mode disabled
		0X1X	Lock to disc mode enabled
		0XX0	Motor brakes to 12%
		0XX1	Motor brakes to 6%

16. CD-graphics interface register

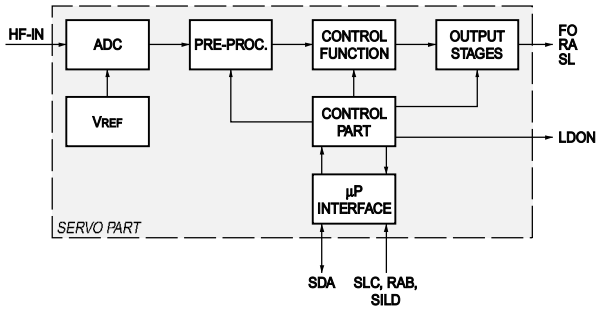
REGISTER	ADDR.	DATA	FUNCTION
CD-graphics interface	1111	X0XX	CD-graphics interface off
		X1XX	CD-graphics interface on
		0XXX	4-wire CD-graphics subcode
		1XXX	3-wire CD-graphics subcode

FUNCTIONAL DESCRIPTION DIGITAL SERVO PART

The digital servo part of the CD7 has the following features:

- Diode signal processing
- Signal conditioning
- Focus and radial control system
- Access control
- Sledge control
- Shock detector
- Defect detector
- Off-track counting & detection
- Hi-level features

Data flow within the servo part



For details about signal processing in digital servo controllers see chapter "Functional description TDA1301T" of booklet "Portable CD ´94".

Output stages

The control signals RA (radial error), FO (focus error) and SL (slide error) are pulse density modulated. The modulation frequency can be set to either 1.0584MHz or 2.1168MHz. An analog representation of the output signals can be achieved by connecting a first order low pass filter to the outputs.

Laser interface

The LDON pin (open drain) is used to switch the laser on and off. When the laser is on the output is HIGH impedance. The pin is automatically driven if the focus control loop is switched on.

Hi-level features

The CD7 includes a number of "Hi-level features". These are extra functions provided to make the application of the device easier, reduce the amount of software, and reduce the amount of time the µP spends monitoring for play errors, etc. Most of the hi-level features may be disabled if they are not required.

The hi-level features implemented in CD7 are:

- Autosequencers
  - Start/restart autosequencer
  - Stop autosequencer
- System watchdogs
  - Focus watchdog
  - Radial play watchdog
  - Radial jump watchdog
  - Subcode discontinuity checker
- Servo AGCs

Start/restart autosequencer

In order to move the system from an idle state (e.g. standby) to a state where it can start to acquire data from the disc, there are a number of actions to be performed. The servos must be activated in a controlled way and continuously monitored for error conditions. This process called "startup". The actions required for a typical startup are as follows:

1. The focus servo is switched on. The servo ramps the focus actuator until the focus point is found. The system must wait until focus is achieved before it can take any further actions.
2. Once in focus, the turntable motor can be started. The motor control relies on a HF-signal from the CD in order to regulate the disc speed. At rest there is no HF-signal, so acceleration of the motor must be done in two phases. In the first phase a fixed forward acceleration voltage is applied to the turntable motor. This is done for a fixed time duration (normally 100...300ms) in order to "kick" the disc sufficiently so that there is a HF-signal and the decoder DPLL can lock to.
   In the second phase the disc is accelerated to 75% of nominal speed. When 75% speed is reached, the decoder automatically switches the motor to jump-mode.
3. The radial scaling mechanism is invoked. It is only necessary to perform this function during the startup of a new disc. Radial scaling must be done when the CD is turning at or close to nominal speed.
4. The radial servo is switched on. The radial servo may only be turned on if the disc is spinning. This is done by issuing a short jump command of approximately 10 tracks.

When the above actions are completed the system should be tracking the data spiral on the disc.
The start/restart sequencer provides steps 1...4 within a state-machine that is invoked with a single 3-byte command.

Focus watchdog

The focus watchdog continuously monitors the focus state of the system. When a focus drop-out of longer than 3ms is detected, following actions are taken:

1. The radial servo is set to hold mode. This avoids skating of the lightpen towards the endpositions.
2. The turntable motor is switched off. This gives the system the opportunity to recover the dropout and restart the servos with a minimum of disruption to the disc speed.
3. The focus servo remains active in ramp mode so focus can be recovered.

Radial play watchdog

The radial play watchdog is a subcode timeout mechanism. It becomes active when the lightpen is on track and a first packet of subcode has been acquired by the decoder.
If the CD7 cannot obtain a new packet of subcode within the time specified by the internal PLAY_WATCH_TIME parameter (programmable), a radial error is reported.
If the radial play watchdog is enabled, the radial servo is switched off to avoid possible damage to the mechanism. The slide motor is put into jump mode.
If the radial play watchdog is disabled, the radial error is still reported, but the radial servo is not switched off. The slide motor remains in play mode.

Radial jump watchdog

The radial jump watchdog is a timeout mechanism for monitoring the offtrack counter. It becomes active after a jump command, when the offtrack counter is loaded with the jump size.

During access the value of the offtrack counter is read every JUMP_WATCH_TIME milliseconds (time is programmable, max. 32ms). Whenever the count changes by less than 4 tracks (e.g. radial skate) a radial error is reported.
If the radial jump watchdog is enabled, the jump is cancelled by switching off the radial servo to avoid possible damage of the mechanism. The slide motor is put into jump mode.
If the radial jump watchdog is disabled, the radial error is still reported, but the radial servo is not switched off. The slide motor remains in play mode.

Subcode discontinuity checker

The subcode discontinuity checker is only active when the internal interface of the CD7 is enabled. It monitors the time field in the Q-subcode information, obtained by the decoder part of the CD7. Q-subcode discontinuity is assumed if:

- New subcode time is before previous subcode time.
- New subcode time is more than 10 frames later than previous subcode time and no subcode timeout has occurred.

When discontinuity is detected, the SUBCODE_DISCONTIN flag in the interrupt status register is set.

Servo AGCs

The CD7 includes automatic gain adjustment procedures for the focus and the radial control loop. The servo AGCs eliminate tolerances in the control loops and should be re-adjusted when starting a new disc.

The procedure for using the servo AGCs is as follows:

1. Start the system with the default settings
2. Write desired injection frequency to internal AGC register.
3. Monitor the AGC_GAIN coefficient until the value has settled.

If the gain value does not settle sufficiently (e.g. due to defect on disc), the AGC should be turned off and the servo parameters reprogrammed with the default values.

The Hi-level feature status can be checked via three internal registers:

1. Interrupt status register

REGISTER	DATA	MEANING
Interrupt status	XXXX XXX1	Focus lost
	XXXX XX1X	Subcode ready
	XXXX X1XX	Subcode absol. sec. changed
	XXXX 1XXX	Subcode discontinuity
	XXX1 XXXX	Radial error
	XX1X XXXX	Autosequencer state change
	X1XX XXXX	Autosequencer error

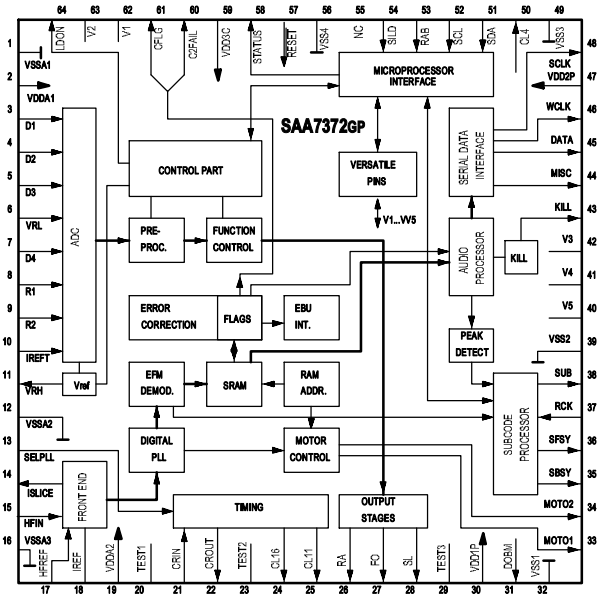
2. Decoder status register

REGISTER	DATA	MEANING
Decoder status	X1XX XXXX	MOTSTART1
	XX1X XXXX	MOTSTART2
	XXX1 XXXX	MOTSTOP
	XXXX 1XXX	PLL LOCK
	XXX1 X1XX	V1
	XXXX XX1X	V2
	XXXX XXX1	MOTOR-OV

3. Autosequencer status register

REGISTER	DATA	MEANING
Autosequencer status	000X 0000	Off mode, no error
	000X 0010	Off mode after focus error
	000X 0100	Off mode after motor start err.
	000X 1000	Off mode after motor stop
	100X XXXX	Focus ramp active, wait
	101X XXXX	Motor in start mode1
	110X XXXX	Motor in start mode2
	111X XXXX	Radial initialization is busy
	010X XXXX	Brake mode

Block diagram and pin configuration



Pin	Name	Description
1	VSSA1	supply (analog) of CD7
2	VDDA1	supply (analog) of CD7
3	D1	unipolar current input (central diode)
4	D2	unipolar current input (central diode)
5	D3	unipolar current input (central diode)
6	VRL	reference input for ADC
7	D4	unipolar current input (central diode)
8	R1	unipolar current input (satellite diode)
9	R2	unipolar current input (satellite diode)
10	IREFT	current reference for calibration ADC
11	VRH	reference output from ADC
12	VSSA2	supply (analog) of CD7
13	SELPLL	selects whether internal clock multiplier PLL is used
14	ISLICE	current feedback from data slicer
15	HFIN	comparator signal input
16	VSSA3	supply (analog) of CD7
17	HFREF	comparator common mode input
18	IREF	reference current pin (nom. VDD/2)
19	VDDA2	supply (analog) of CD7
20	TEST1	test control input
21	CRIN	crystal/resonator input
22	CDOUT	crystal/resonator output
23	TEST2	test control input
24	CL16	16.9344MHz system clock output
25	CL11	11.2896MHz or 5.6448MHz clock output
26	RA	radial actuator output
27	FO	focus actuator output
28	SL	slide actuator output
29	TEST3	test control input
30	VDD1P	supply (digital) of CD7
31	DOBM	digital bi-phase mark output (3-state)
32	VSS1	supply (digital) of CD7
33	MOTO1	motor output1 of CD7; versatile (3-state)
34	MOTO2	motor output2 of CD7; versatile (3-state)
35	SBSY	subcode block sync (3-state)
36	SFSY	subcode frame sync (3-state)
37	RCK	subcode clock input
38	SUB	P to W subcode bits (3-state)
39	VSS2	supply (digital) of CD7
40	V5	versatile output pin of CD7
41	V4	versatile output pin of CD7
42	V3	versatile output pin of CD7 (open drain)
43	KILL	kill output; programmable (open drain)
44	MISC	C2 error flag; output only defined in CD-ROM modes (3-state)
45	DATA	serial data output (3-state)
46	WCLK	word clock output (3-state)
47	VDD2P	supply (digital) of CD7
48	SCLK	serial bit clock output (3-state)
49	VSS3	supply (digital) of CD7
50	CL4	4.2336MHz µP clock output
51	SDA	µP interface data I/O line (open drain output)
52	SCL	µP interface clock line
53	RAB	µP interface R/W and load control line
54	SILD	µP interface R/W and load control line
55	NC	no connection
56	VSS4	supply (digital) of CD7
57	RESET	power-on reset input (active low)
58	STATUS	servo interrupt request line/ CD7 status register output (open drain)
59	VDD3C	supply core (digital)
60	C2FAIL	indication of correction failure (open drain)
61	CFLG	correction flag output (open drain)
62	V1	versatile input pin
63	V2	versatile input pin
64	LDON	laser drive on output (open drain)

SM5856A1F – ANTI-SHOCK MEMORY CONTROLLER "NPC"

GENERAL DESCRIPTION

The NPC is a compression-type anti-shock memory controller LSI for compact disc players. It is used to make the player insensitive to mechanical shocks. This is done via an external DRAM, which is filled-up with audio data at twice the normal speed. If a shock occurs data of the DRAM is played, while the set is recovering from the shock.
In contrast to "ordinary" memory controllers the NPC is able to store audio data in compressed form (ADPCM-algorithm). This increases the audio capacity of the external DRAM. The NPC can handle different compression rates and DRAM-sizes, what make the IC attractive for a wide range of applications.

FUNCTIONAL DESCRIPTION

The NPC has two modes of operation:
• bypass mode
• shock-proof mode

Bypass mode

In bypass mode the NPC does not perform any shock-proof functions. Audio data passes only the attenuator and mute sections of the IC. The external DRAM is not accessed. In bypass mode the input rate is fixed to fs, synchronized to the system clock of 384fs.

Shock-proof mode

The shock-proof mode makes the player insensitive to mechanical shocks. During playback following three sequences are encountered:

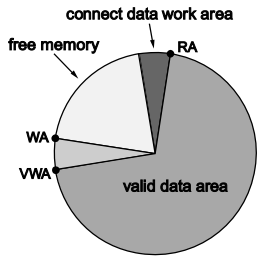
1. Encoding sequence
• Input data from the CD-decoder is stored in internal buffers.
• Encoding starts after a fixed number of audio data has been received. The encoding algorithm is optimized for most suitable prediction filter type and quantization steps.
• Encoded ADPCM-data is stored in the external DRAM.

2. Decoding sequence
• ADPCM-data is read from the external DRAM with rate fs.
• Decoding starts with prediction filter type and quantization level, used for encoding.
• Attenuation and muting operation is performed if required.
• Audio samples are fed to the audio output interface.

3. Compare-connect sequence
• Encoding is stopped immediately if either external DRAM overflows or read errors occur due to shock vibrations.
• The compare-connect start command is executed and compare-connect sequence starts.
• Re-read data from the CD is compared with the data stored in the DRAM.
• As soon as the comparison algorithm detects conforming data, compare-connect is stopped and encode sequence re-starts. Re-read data is connected directly behind the previous valid data.

RAM addresses

The NPC uses either one or two 1Mbit or 4Mbit DRAMs as external data buffers.
The available memory is split-up into four areas, separated by the address pointers
WA (Write Address),
VWA (Valid Write Address) and
RA (Read Address).



Write data area
The write data area contains audio data, whose validity has not been confirmed, yet. The address pointer WA marks the next (free) memory position, where write actions to the memory can take place.

Valid data area
The valid data area contains confirmed audio data. Only valid data is forward to the audio output interface.

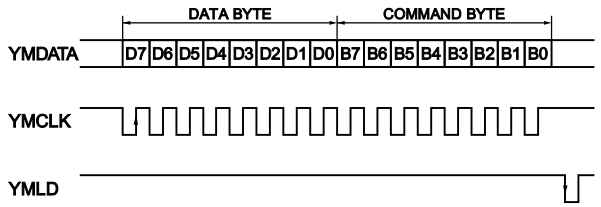
Connect data work area
The connect data work area is a reserved memory, used by the compare-connect sequence. The size of this area is fixed and depends on the capacity of the external DRAM. It is 2kbits if using 1Mbit DRAMs, or 4kbits if using 4Mbit DRAMs.

Free memory
This area does not contain any data, yet.

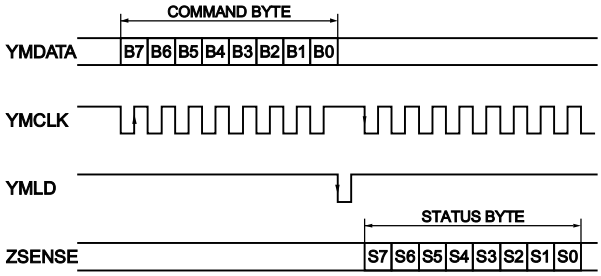
Microcontroller interface

The NPC has a three line serial interface for data transfer to and from the µP. The interface consists of
YMDATA .....data line
YMCLK.....bit clock
YMLD .....load signal

Write operation sequence

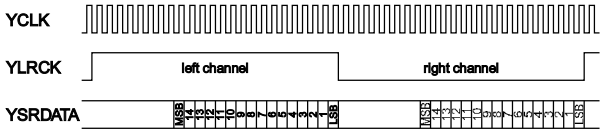


Read operation sequence



Audio input interface

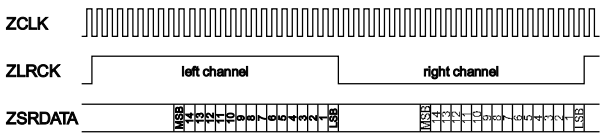
The audio input interface consists of three wires.



In shock-proof mode the input rate of the audio data must be within 0...2 times the normal audio signal rate.
In bypass mode the input rate is exactly the normal audio signal rate, the interface is synchronized with the 384fs system clock input CLK.

Audio output interface

The audio output interface consists of three wires.



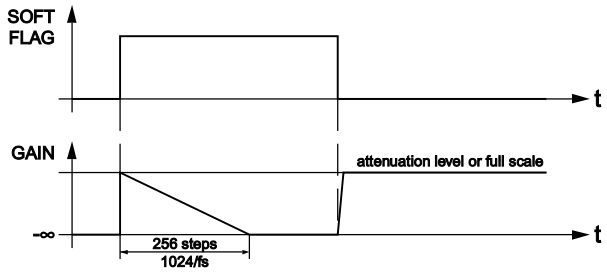
The output rate of the audio data is the normal audio signal rate fs. It is synchronized to the 384fs system clock input.

Attenuation

Attenuation is controlled by the ATT-flag (command register) and the ATT-value (attenuation register).
When the ATT-flag is 1 attenuation is carried out. The gain depends on the ATT-value and is calculated with
Gain = 20 * log (ATT – value/256) [dB].
When the ATT-value or ATT-flag changes, the gain moves smoothly from the previous set gain towards the new set value. The gain changes with a rate of 4/fs per step.

Soft mute

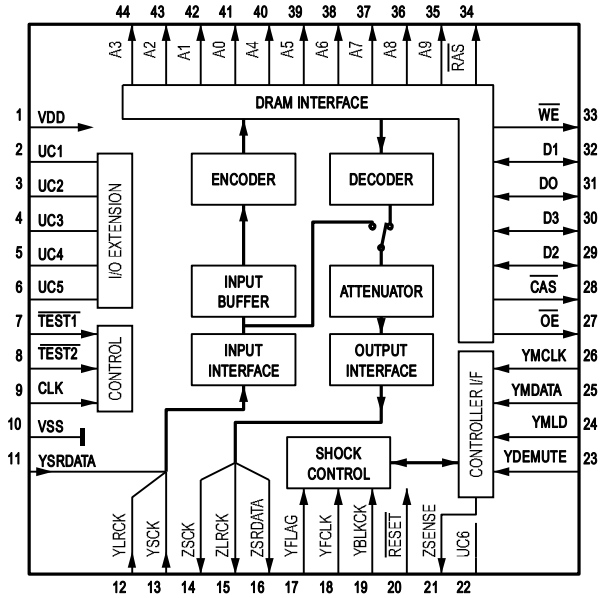
Soft mute operation is controlled by the SOFT-flag (command register) using a built-in attenuation counter. Mute is on when the SOFT-flag is 1. When on, the attenuation counter output is decremented in steps of 1, thereby reducing the gain. A complete mute takes 1024/fs (or approximately 23.2ms at fs=44.1kHz).
Conversely mute is released when the SOFT-flag is 0. In this case the attenuation counter is immediately set to the value when the ATT-flag was 1. If the ATT-flag was 0, the new set value is 256 (0dB).



Force mute

Serial data output is muted by setting the YDMUTE input pin to HIGH or by setting the MUTE-flag to 1. Mute starts and finishes on the leading left-channel bit.

Block diagram and pin configuration



Pin	Name	Description
1	VDD	supply voltage
2	UC1	µP interface extension I/O line 1
3	UC2	µP interface extension I/O line 2
4	UC3	µP interface extension I/O line 3
5	UC4	µP interface extension I/O line 4
6	UC5	µP interface extension I/O line 5
7	NTEST1	test input1
8	NTEST2	test input2
9	CLK	16.9344MHz clock input
10	VSS	ground
11	YSRDATA	audio serial data input
12	YLRCK	audio serial L/R clock input
13	YSCK	audio serial bit clock input
14	ZSCK	audio serial bit clock output
15	ZLRCK	audio serial L/R clock output
16	ZSRDATA	audio serial data output
17	YFLAG	signal processor IC RAM overflow flag
18	YFCLK	crystal-controlled frame clock input
19	YBLKCK	subcode block clock signal output
20	RESET	system reset input (active low)
21	ZSENSE	µP interface status output
22	UC6	µP interface extension I/O line6
23	YDMUTE	forced mute input
24	YMLD	µP interface latch clock input
25	YMDATA	µP interface serial data input
26	YMCLK	µP interface shift clock input
27	OE	DRAM OE control output (active low)
28	CAS	DRAM CAS control output (active low)
29	D2	DRAM data input/output 2
30	D3	DRAM data input/output 3
31	D0	DRAM data input/output 0
32	D1	DRAM data input/output 1
33	WE	DRAM WE control output (active low)
34	RAS	DRAM RAS control output (active low)
35	A9	DRAM address output 9
36	A8	DRAM address output 8
37	A7	DRAM address output 7
38	A6	DRAM address output 6
39	A5	DRAM address output 5
40	A4	DRAM address output 4
41	A0	DRAM address output 0
42	A1	DRAM address output 1
43	A2	DRAM address output 2
44	A3	DRAM address output 3

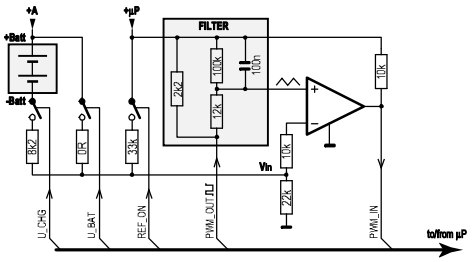
BATTERY CHARGING

BASIC CONSIDERATIONS

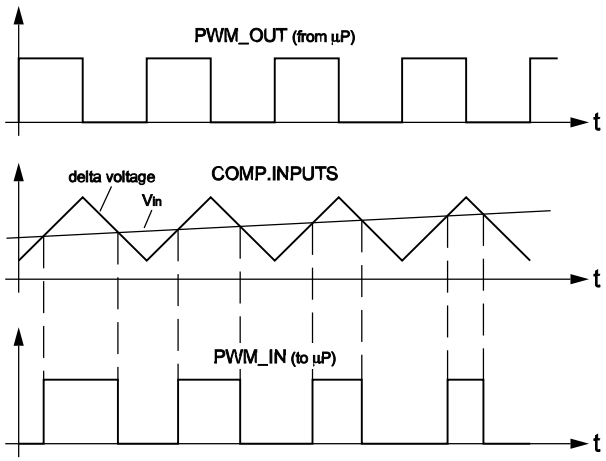
In the design phase of the CD-portable range 1996 the wish for a charge function for both, NiCd and NiMH batteries, came up. Investigations had shown that NiMH batteries should not be overcharged for more than 150% of their charge capacity. Therefore simply charging over a fixed period of time was no solution for that problem – a more "intelligent" charge circuit was required.
In order to ensure proper charging and lifetime of the batteries the battery voltage must be constantly measured over the whole charging time.
As criterion for switching off the charge current following observation was used: The battery voltage decreases after the maximum charge capacity has been reached. Unfortunately the decrease is very small (5...10mV). Assuming a maximum battery voltage of 3V the voltage drop to be measured is in the range of 0.16...0.33% ! As a result the battery voltage has to be measured with a resolution in the mV range. Since ADCs with that accuracy are rather expensive, a PWM-ADC was implemented.

PWM-ADC

The PWM-ADC consists of a comparator, a filter and the µP.



The µP generates a PWM-signal at the output pin PWM_OUT. This signal passes a filter, yielding a delta signal with a certain DC-level. The DC-level depends directly on the duty cycle of the PWM-signal.
The comparator compares the triangle shaped signal with Vin (the voltage to be measured). At the comparator´s output a rectangular signal is formed, which is HIGH for the time the delta voltage is higher than Vin and LOW for the time the delta voltage is lower than Vin.



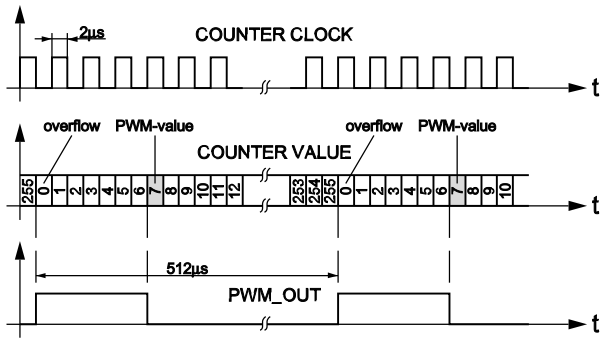
Now the comparator output high time is measured. This is done by an internal counter of the µP. The parameters duty cycle and high time are a measure for the unknown voltage Vin. If Vin leaves the range of the delta voltage, the duty cycle of the PWM-signal has to be re-adjusted (see section "Adjustment of PWM-value").

Generation of PWM-signal

As already mentioned the PWM-signal is generated by an internal counter of the µP. This counter has a resolution of 8-bit, what allows 256 PWM-steps. The actual PWM-value (= duty cycle) is stored in an internal 8-bit register.
The counter frequency is set to 1/8 of the external clock and calculated with $f_{counter}$ = 4MHz/8 = 500kHz.

PWM-pulses are created as follows:

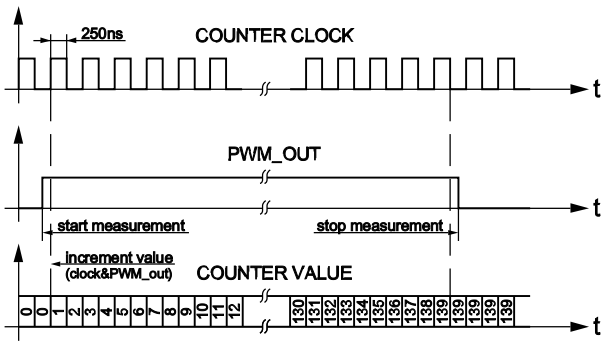
- PWM_OUT is initially set HIGH.
- The counter counts up every 2µs (1/500kHz) until the PWM-value, stored in the internal register, is reached.
- PWM_OUT is now switched to LOW, until a counter overflow occurs (increment at 255).
- The counter is cleared and PWM_OUT becomes HIGH again.



One PWM-cycle takes 256*2µs = 512µs, what results in a PWM-frequency of 1/512µs = 1.95kHz.

Measurement of comparator high time

The measurement of the comparator output high time is achieved by another counter of the µP.
Based on a clock frequency of 4MHz the resolution of the measurement is 1/4MHz = 250ns.
PWM_IN is logically AND-ed with the internal clock. The counter starts on the rising edge and stops on the falling edge of this AND-ed product.



The counter value is read from an internal 16-bit register. Counter value multiplied by 250 gives the comparator output high time in [ns].

Approximately every second a measurement takes place. Alternatively +Batt (reference voltage) and -Batt (battery voltage) are measured. After 15+15 samples (approximately 60 seconds) an average value for t_{REF} and t_{BAT} and the difference of these values (Δt) are calculated (additional two factors are served by the PWM adjustment procedure). The differences of the Δt-values are summed up over a measurement period of 15 minutes. The resulting values Δt_{REF} and Δt_{BAT} correspond to the drift of the reference voltage respectively the slope of the battery voltage, and are an input for the switch off criterion detection (described later in this chapter).

In practice additional measures are implemented to increase the immunity against erroneous measurement, caused by bursts, ESD, voltage drift, a.s.o. Because these measures do not effect the basic working principle, they should not be subject of this description.

Adjustment of PWM-value

As it is possible that the voltage to be measured moves out of the range of the delta voltage, the comparator output would be in a steady HIGH or steady LOW state. In this case the duty cycle of the PWM_OUT signal (means the PWM-value) must be re-adjusted. This is realized by a so-called "detection window". Whenever the measured comparator output high time moves out of the valid range of 156µs < t_{PWM_IN} < 356µs a re-adjustment of the PWM-value takes place. This is done by simply incrementing / decrementing the PWM-register. The PWM-value is

- decremented by 2 if PWM_IN is ≤ 156µs
- incremented by 2 if PWM_IN is ≥ 356µs

Incrementing / decrementing is repeated as long as PWM_IN comes back into the valid window.

Switch off criterion detection

Depending on the summed-up Δt-values of t_{REF} and t_{BAT} (see section "Measurement of comparator high time") further actions are encountered:

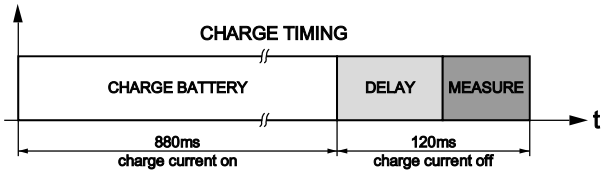
CONDITION	ACTION
Δt_{ref} > 8µs	*too high voltage drift of reference voltage* → continue charging and restart measurements,
Δt_{bat} > 10µs	*switch off criterion fulfilled* → stop charging and enter trickle charge
0µs≥Δt_{bat}≤10µs	*switch off not fulfilled, but batteries almost full* → continue charging and test switch off criterio Δt_{bat} > 10µs
Δt_{bat} < 0µs	*switch off criterion not fulfilled* → continue charging, reset measurements and

In addition total charging time and battery temperature are monitored continuously. Following conditions immediately stop respectively interrupt the charging process:

CONDITION	ACTION
total charging time > 7h	*switch off criterion fulfilled* → stop charging and enter trickle charge
battery temperature > 50° C	→ interrupt charging until temperature is low a → continue charging and restart measurements

Charge timing

An important detail was not discussed, yet – the charge timing. As described earlier measurements take place every second. In order to achieve stable conditions for the measuring part, the charge current can´t be switched on permanently. One second of the charge process must therefore be split-up into three phases:



1. Charge phase (880ms)

In this phase the charge current is switched on.
The battery is charged with an average current of
$I_{average} = I_{const} * 880ms/1000ms = 300mA * 0.88 = 264mA$.

2. Delay time

During the delay time the charge current is switched off. This ensures stable conditions for the measuring part.

3. Measurement phase

Measurements are carried out during the last section of the charge off phase.

Trickle charge

After batteries are charged trickle mode is entered. In this state the charge current is switched on for 40ms and switched off for 680ms, periodically. This prevents the batteries from being self-discharged. The trickle mode is also activated in standby mode.

Trickle mode is only stopped if

- the user leaves standby mode (e.g. PLAY)
- the AC/DC-adapter is unplugged
- the accu pack is removed (accu pack switch not closed)
- the batteries get too hot
  Remark: After the temperature was LOW again for 30 minutes trickle charge is continued.

DC/DC-CONVERTER

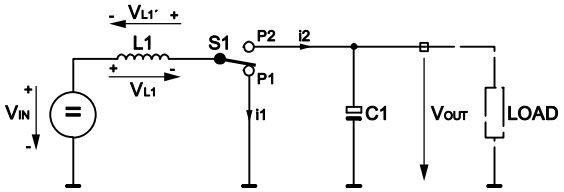
BASIC CONSIDERATIONS

The portable CD-range 1996 is the first family using a 2-battery concept. This means, compared to the 4-battery solution of the predecessors, only half of the battery capacity and thus only half of the playing time.
In order to ensure acceptable life time of batteries the electronics have been optimized for low power consumption. The main improvements are covered by the new CD-drive CDM12.3BLC, use of CD7 and a re-design of the DC/DC-converter.

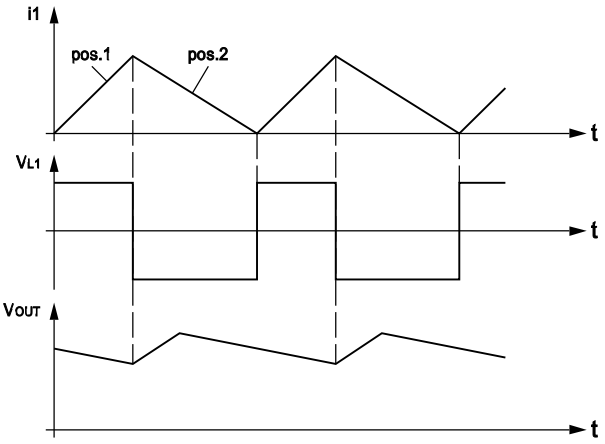
The DC/DC-converter of a portable CD-player must meet following requirements:
- Upconversion of battery voltage with high efficiency
- Minimum components (printed board space and cost)

WORKING PRINCIPLE OF A DC/DC-UPCONVERTER

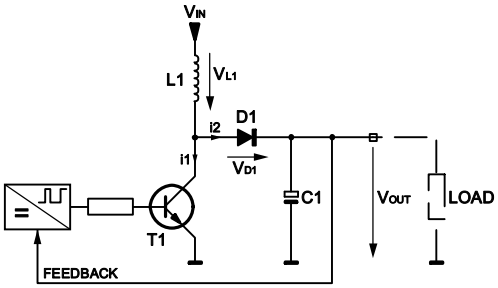
A standard DC/DC-upconverter consists of three elements: Reversing switch S1, coil L1 and capacitor C1.
The basic circuit diagram is given below:



In position P1 a current i1 flows from V_{IN} through the coil to ground. L1 is "charged" with $\Delta i \approx V_{IN} * \Delta t/L$.
At the moment S1 is switched to position P2 the inducted voltage V_{L1} at the coil changes its polarity (L1 tries to keep i1 constant). The energy, stored in L1 charges the capacitor with $\Delta i \approx (V_{OUT} - V_{IN}) * \Delta t/L$.
As the (now reversed) inducted voltage $V_{L1'}$ is added to V_{IN}, the output voltage V_{OUT} is higher than the input voltage.



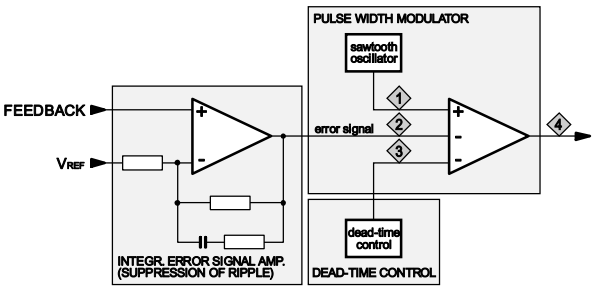
In practice the reversing switch is formed by a transistor and a diode. The on/off-timing for the transistor is generated by a separate feedback loop (described in next paragraph).
The resulting circuit diagram is as follows:



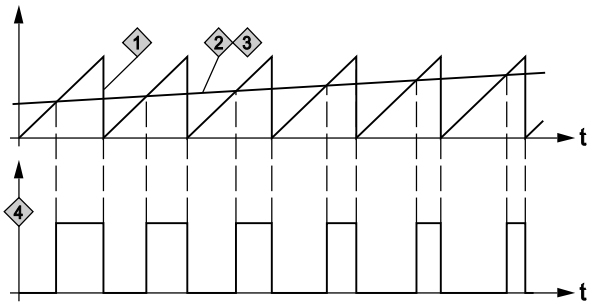
It can be seen that whenever the base of T1 is HIGH the transistor switches through and L1 is charged. Diode D1 blocks discharge of C1 to ground (i2 = 0).
When the base of T1 goes LOW a current i2 charges C1 via V_{IN}, L1 and D1. The output voltages is calculated with $V_{OUT} \approx V_{IN} + V_{L1} - V_{D1}$.

GENERATION OF CONTROL SIGNAL

The control signal for T1 is generated by an integrating error signal amplifier and a pulse width modulator. The modulator consists of a sawtooth oscillator and a comparator.
An additional circuitry, the so-called "dead-time control", defines a minimum switch off time in order to limit the current through the coil. The blockdiagram is given below:



The feedback voltage is integrated by the error signal amplifier and fed forward to the inverting input of a comparator. The comparator now compares this signal with the output of the sawtooth oscillator. At the comparator´s output a rectangular signal is formed, which is HIGH for the time the sawtooth voltage is higher than the error signal and LOW for the time the sawtooth voltage is lower than the error signal.



Dependent on the value of the error signal the duty cycle of the rectangular signal changes. The output of the comparator directly controls the on/off-time of transistor T1 and thus the current flow through the coil. In case of higher demand of output current the control loop increases the on-time of T1 and more energy is stored in the coil respectively charged into the capacitor. In case of lower output currents the off-time increases and less energy reaches the capacitor.

Dead-time control

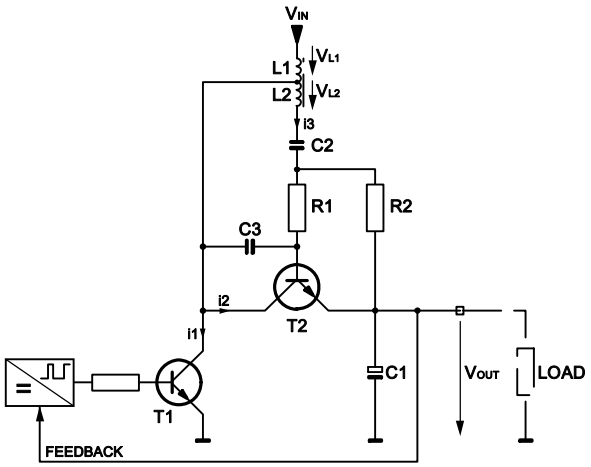
Whenever capacitor C1 is completely discharged (e.g. at start-up) the feedback voltage becomes zero. Consequently the output of the comparator would always be HIGH because the feedback voltage is always lower than the sawtooth signal. Also transistor T1 would always be switched through and the coil could never be “discharged”.
The dead-time control now simply adds a certain DC-offset to the feedback signal in order to ensure a minimum duty cycle at the comparator´s output. This measure also limits the maximum current through the coil ($V_{MAX} = V_{IN} * t_{on}/L$).

IMPROVEMENTS OF STANDARD UPCONVERTER

The previously described standard DC/DC-upconverter has three disadvantages:

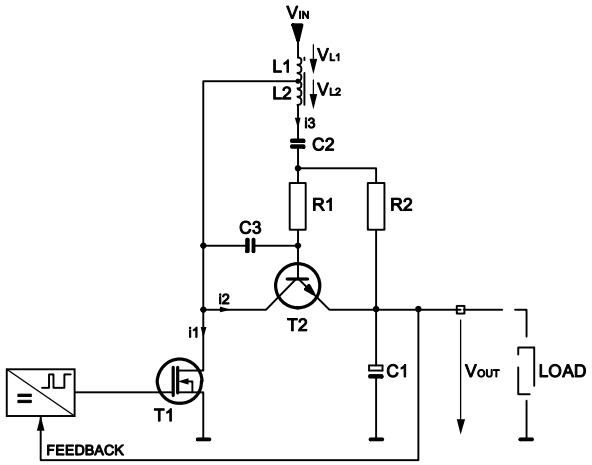
- Voltage drop at diode D1
- No power-off function
  (permanent current flow from V_{IN} via L1 and D1 to load)
- Base current of T1 is lost

1. Modification for minimum voltage drop and power-off



For minimum voltage drop diode D1 is replaced by transistor T2. In order to fulfil the switching criterion the base of the transistor must become higher than the emitter. The easiest way to achieve that is to use a transformer instead of a single coil.
When the base of T1 is HIGH the transistor switches through and L1 is charged. The inducted voltage at L2 pushes the base of T2 to lower potential than V_{OUT} and T2 is blocked. When the base of T1 goes low the transistor is blocked. The inducted voltages V_{L1} and V_{L2} change polarity and are added to V_{IN}. T2 switches through and C1 is charged by i2 and i3. The additional components C3 and R2 improve the switching behaviour.
For the power-off function components R1/C2 are built-in. In order to switch off the DC/DC-converter the base of T1 is kept LOW. C1 is discharged by the load. As soon as the output voltage V_{OUT} becomes lower than V_{IN} capacitor C2 is charged via V_{IN}, L1, L2, R1 and T2. When the voltage at C2 reaches V_{IN} the base-emitter voltage of T2 becomes zero and the transistor blocks. As a result also the current flow from V_{IN} to the load is blocked – the circuitry is switched off.

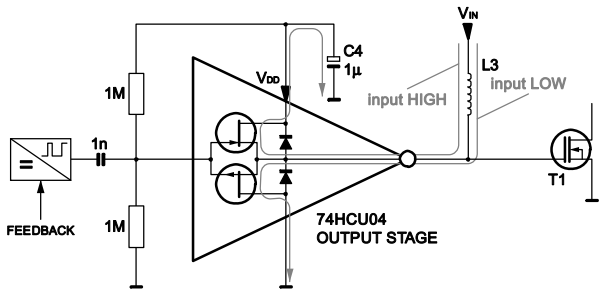
2. Modification for saving base current of T1



For saving base current the bipolar transistor T1 is replaced by a field effect transistor (advantage: nearly wattless control). However, compared to the bipolar type the FET requires a relatively high control voltage at the gate.
The upconversion of the gate voltage is covered by a voltage doubler.

Voltage doubler

The voltage doubler in use is built-up with the inverter stage of an ordinary 74HCU04 device.

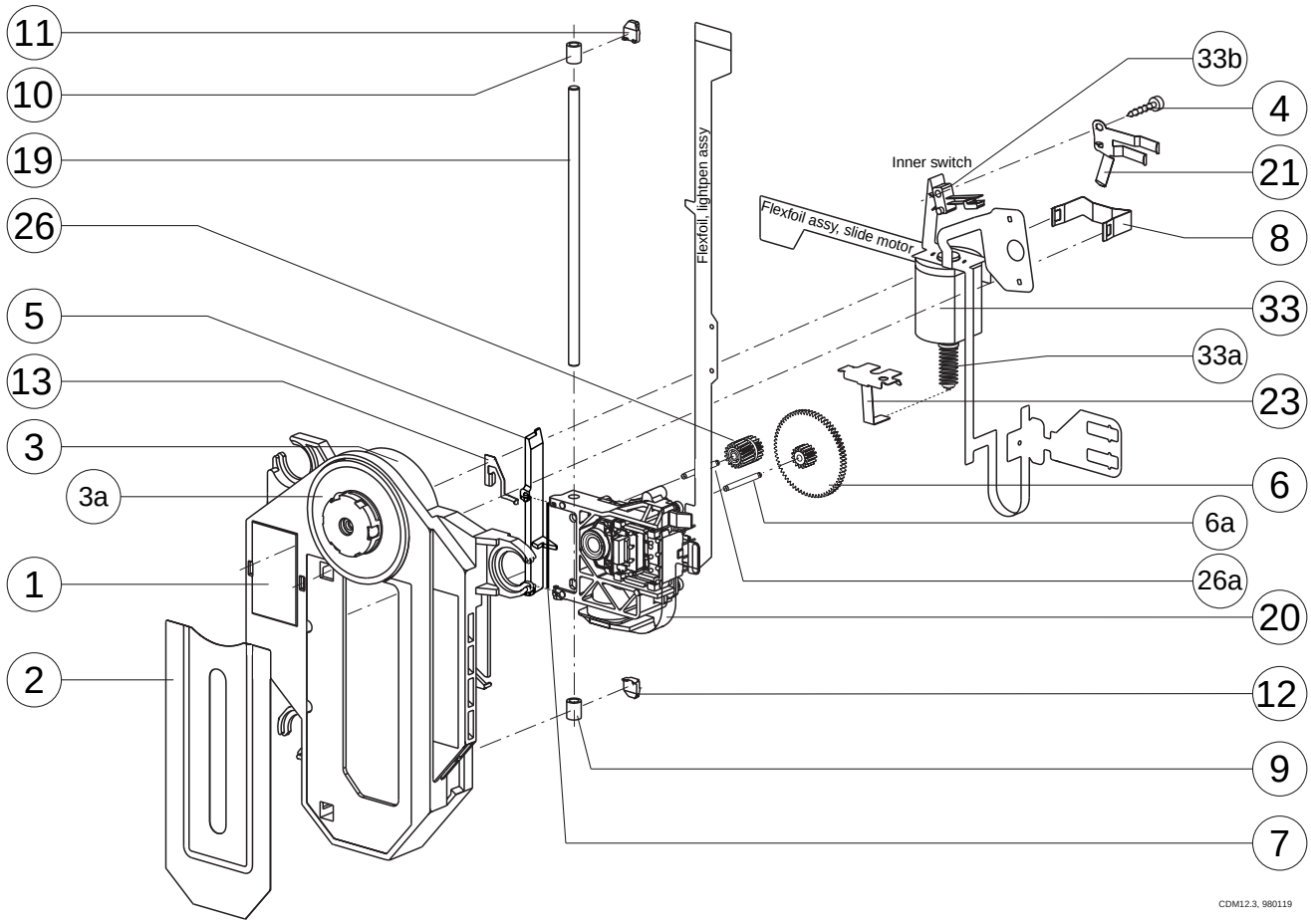


The input of the inverter is triggered by the same rectangular voltage, used for DC/DC-upconversion. Capacitor and voltage divider at the input couple in the rectangular voltage at $V_{DD}/2$. This measure ensures switching independent on the supply voltage of the device. With every rising edge the lower FET of the output stage switches through. Current flows via V_{IN}, coil and FET to ground – energy is stored in the coil L3.
With every falling edge the upper FET of the output stage switches through. At the output the (now reversed) inducted voltage at the coil is added to V_{IN}. Current flows from V_{IN} via L3 and upper FET into C4 – the capacitor is charged to nearly twice the input voltage.
The really trick behind this circuitry is that the device generates its own supply voltage V_{DD}.

ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ADC	Analog to Digital Converter
ADPCM	ADaptive Pulse Code Modulation
AGC	Automatic Gain Control
ALPC	Automatic Laser Power Control
CAV	Constant Angular Velocity
CD	Compact Disc
CD7	Compact Disc decoder&digital servo integrated circuit, 7th generation
CDM	Compact Disc Mechanism
CIRC	Cross Interleaved Reed Solomon Code
CLK	CLocK (frequency)
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DC	Direct Current
DOBM	Digital Output Biphase Mark
DPLL	Digital Phase-Locked Loop
DSIC2	Digital Servo Integrated Circuit, 2nd generation
EBU	European Broadcasting Union
EFM	Eight to Fourteen Modulation
EIAJ	Electronic Industries Association of Japan
ESA	Electronic Shock Absorption
ESD	ElectroStatic Discharge
ESP	Electronic Skip Protection
FET	Field Effect Transistor
FIFO	First In First Out
fs	Sampling Frequency
GND	GrouND
HF	High Frequency
IC	Integrated Circuit
IEC	International Electrotechnical Commission
I/F	InterFace
I/O	Input/Output
LASER	Light Amplification by Stimulated Emission of Radiation
LDGU	Laser Diode Grating Unit
LSB	Least Significant Bit
LSI	Large Scale Integration
MSB	Most Significant Bit
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
RL2	Run Length 2
RL3	Run Length 3
ROM	Read Only Memory
R/W	Read/Write
VCO	Voltage Controlled Oscillator

COMPACT DISC DRIVE CDM12.3BLC – 4822 691 10487



TECHNICAL SPECIFICATION CDM12.3BLC

Focus/radial tracking actuator	**CDM12.3BLC**
Working area:	
focus	±0.5mm
radial tracking	0.35mm min.
DC sensitivity:	
focus	1mm/V ±20%
radial tracking	0.24mm/V ±20%
AC sensitivity (200Hz):	
focus	0.16N/A ±20%
radial tracking	0.25N/A ±20%
Resonance frequency:	
focus	30Hz +7Hz
radial tracking	49Hz ±5Hz
Coil resistance:	
focus	7.1Ω ±15%
radial tracking	18Ω ±15%
Laser diode	
Laser wavelength (30°C)	780nm ±20nm
Max. power intensity out of lens	≤0.5mW
Nom. laser current	36mA (47mA max.)
Slide motor	
Motor type	FF-030PK-08250
Resistance (20°C)	13.8Ω ±10%
Starting voltage in application	0.6V typ. (1.2V max.)
Disc readout diameter	47.4...117.5mm
Turntable motor	
Motor type	RF-410CH-12250
Resistance (20°C)	5.7Ω ±8%
Operating voltage in application	0.5V typ.

PARTSLIST

1	Mounting plate assy	11	Clamping plate (spindle)
2	Ornam. plate assy	12	Clamping plate (spindle)
3	Turntable + motor	13	Contact spring (earth)
3a	Turntable	19	Spindle
4	Screw M1.6x8 Torx	20	Light pen assembly
5	Guide block (toothed bar)	21	Earth spring
6	Gearwheel	23	Pivot spring
6a	Spindle	26	Idler wheel
7	Spring wire	26a	Spindle
8	Clamping bracket	33	Slide motor assembly
9	Sleeve (spindle)	33a	Wormwheel
10	Sleeve (spindle)	33b	Inner switch

Remark: The CDM12.3BLC is only available as complete assembly, and as such not repaired. This sheet is published for standardized descriptions of failure causes, only.

HANDLING RECOMMENDATIONS

- Storage in dusty environments should be avoided.
- To avoid damage of the light pen assembly by electrostatic discharges, measuring equipment and operators must be grounded during handling.
- Contamination of the objective lens will influence the performance. Avoid fingerprints on the lens.
- The actuator with lightpath has been adjusted carefully during manufacturing. Avoid high forces on this part. Do not disassemble or re-adjust.
- The laserbeam may damage the human eye. Do not look directly into the objective lens.
- Fast heating up (e.g. by bringing the CDM from a cold place into a warm and humid room) can result in moisture condensating on the lens, thus influencing the playability for a certain time. Before checking the performance the CDM should acclimatize for at least 30 minutes.